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# APPLICATION FOR UNITED STATES LETTERS PATENT

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**FOR:** PRINTED CIRCUIT BOARD, METHOD FOR PRODUCING SAME AND SEMICONDUCTOR DEVICE

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# PRINTED CIRCUIT BOARD, METHOD FOR PRODUCING SAME AND SEMICONDUCTOR DEVICE

[0001]

## FIELD OF THE INVENTION

This invention relates to a printed circuit board and, more particularly, to a printed circuit board having a capacitor structure, a method for producing the same, and to a semiconductor device.

[0002]

## BACKGROUND OF THE INVENTION

In connection with a conventional printed circuit board, having a capacitor buried in a substrate thereof, reference is had to, for example, the following publications:

[0003]

(1) Publication of JP Patent No. 2738590, and

(2) Publication of JP Patent Kokai JP-P2001-320171A.

[0004]

Of these, the publication (1) (Publication of JP Patent No. 2738590) discloses a capacitive printed circuit board including a capacitor laminate and a plural number of devices respectively connected to different portions of the capacitor laminate, in which the capacitor laminate is made up by laminated dielectric sheets and two electrically conductive foils, arranged on both sides of the laminated dielectric sheets, and having a first surface surface-processed to present a surface roughness sufficient to exhibit adhesion to the laminated

dielectric sheets, in which the second surface of each electrically conductive foil opposite to the first surface is surface-processed to present a surface roughness to exhibit adhesion within the capacitive printed circuit board, in which the capacitor laminate is made up by one dielectric sheet and two electrically conductive foils, as the first surface of said electrically conductive foil is tightly contacted with the dielectric sheet and in which the dielectric sheet is of the minimum thickness in all portions thereof facing the electrically conductive foil. Specifically, the above Publication 1 discloses a structure of a capacitor laminate in which electrically conductive layers are arranged on both sides of an organic dielectric layer to operate as a capacitor. However, with this structure, the capacitance cannot exceed the limit of approximately several nF at most.

[0005]

In a well-known manner, there are three techniques for increasing the capacitance C of a capacitor, that is

- increasing the surface area of an electrode;
- reducing the separation between the electrodes (or reducing the thickness of the dielectric layer between the electrodes); and
- increasing the dielectric constant of the dielectric layer.

[0006]

However, in light of product reliability, such as electrical insulating properties, or manufacture process, it is difficult to reduce the film thickness of the dielectric layer to 1 $\mu$m or less. It is similarly difficult to increase the dielectric constant of the dielectric

layer drastically.

[0007]

For increasing the surface area of the electrically conductive layer of the facing capacitive electrodes, the metal surface is roughed to apparently increase the surface area, as described in Publication 1. However, with the technique described in Publication 1, the surface area of the facing electrode surfaces cannot be actually increased, and hence a sufficient performance cannot be achieved.

[0008]

There is also a method of burying a component, operating as a capacitor, in the bulk of the printed circuit board. However, the buried type capacitive component prescribes the substrate thickness or the electrode contact site and thus imposes constraint on the degree of freedom in substrate designing.

[0009]

The second Publication (Publication of JP Patent Kokai JP-P2001-320171A) discloses a structure comprising a dielectric layer for a capacitor, formed of aluminum oxide, which covers the surface of the aluminum substrate, and a plating layer for a capacitor electrode, which is formed to cover the surface of the dielectric layer for the capacitor. The aluminum substrate, the dielectric layer for the capacitor and the plating layer for the capacitor electrode go to make up a capacitor in a multi-layered circuit substrate to eliminate the necessity of embedding a chip capacitor in an inter-layer insulating film to reduce the thickness of the inter-layer insulating film thereby reducing the thickness of the

multi-layered circuit substrate in its entirety. This Publication (2) indicates that a dielectric film for a capacitor of $Al_2O_3$ may be formed by oxidizing the surface of the aluminum substrate with oxygen plasma to form a dielectric film for the capacitor of $Al_2O_3$ as a surface layer or to deposit powders of $Al_2O_3$ on the surface of an aluminum substrate formed by sintering. However, the aluminum oxide film, formed by, for example, sintering of the powders, is not up to the requirement for a reduced thickness.

[0010]

SUMMARY OF THE DISCLOSURE

In the structure of layering the dielectric sheet, disclosed in Publication 1, the thickness of the dielectric sheet cannot exceed several $\mu$ m by physical limitation, so that a capacitance as large as tens of $\mu$ F cannot be realized. Moreover, in the structure shown in Publication 1, the dielectric sheet is sandwiched between electrically conductive foils having roughed surfaces. That is, the surfaces of the both side electrically conductive foils are merely roughed without substantially increasing the surface area of the electrodes. Specifically, the effect of increasing the surfaces of the opposing electrodes cannot be achieved.

[0011]

The structure of Publication 2 also is not up to the requirement for reduction in the film thickness.

[0012]

In view of the above-depicted status of the art, it is an object of the present invention to provide a printed circuit board capable of

accumulating a large amount of electrical charges, a method for producing the printed circuit board, and a semiconductor device provided with the printed circuit board.

[0013]

According to one aspect of the present invention there is provided a printed circuit board comprising a metal sheet having a surface partially or totally roughed, a dielectric film for a capacitor covering at least the roughed surface of the metal sheet, a first electrically conductive layer covering the surface of the dielectric film for the capacitor, a second electrically conductive layer formed on the surface of the first electrically conductive layer and electrically connected to an electrode of a first via for electrical connection to the first electrically conductive layer, and a resin layer provided for encapsulating an assembly made up by the metal sheet, dielectric film for the capacitor, the first electrically conductive layer and the second electrically conductive layer. The first via for connection is formed on boring through the resin layer until reaching the second electrically conductive layer, the first via for connection including a first electrode of a conductive member deposited therein, while the second via for electrical connection to the metal sheet is not provided with the dielectric film for the capacitor, nor with the first electrically conductive layer, nor with the second electrically conductive layer on the metal sheet in the second via for electrical connection to the metal sheet. The second via for connection is formed extending throughout the resin layer until reaching the metal sheet. The second via for connection includes a second electrode of an

electrically conductive member therein. The second electrode is electrically insulated from the first electrically conductive layer by an insulating member provided between the second electrode and the first electrically conductive layer.

[0014]

In the printed circuit board according to the present invention, the dielectric film for the capacitor is formed of a film of a metal oxide.

[0015]

In the printed circuit board according to the present invention, the first electrically conductive layer is formed of an electrically conductive resin which forms a solid electrolyte of a cathode. In the printed circuit board according to the present invention, the electrically conductive resin is preferably at least one electrically conductive high molecular compound selected from the group consisting of polypyrrole, polythiophene and polyaniline.

[0016]

In the printed circuit board according to the present invention, the second electrically conductive layer is of a double-layer structure comprised of a carbon paste layer and a silver paste layer. Alternatively, the second electrically conductive layer in the printed circuit board according to the present invention may be formed of a metal plating layer.

[0017]

In the printed circuit board according to the present invention, the insulating member may be formed of a resin encapsulating the metal

sheet, a dielectric film for the capacitor, a first electrically conductive layer and a second electrically conductive layer, or may be provided different from the encapsulating resin.

[0018]

In another aspect, the present invention provides a semiconductor device comprising a semiconductor chip and the printed circuit board in one aspect of the present invention, wherein the printed circuit board includes a through-hole extending from one surface to the opposite side surface of the printed circuit board, the through-hole including a conductor formed on an inner wall surface thereof. The first and second electrodes, provided in respective vias for connection on one surface of the printed circuit board, are connected to first and second power supply terminals of the semiconductor chip, and signal electrodes of the one surface of the printed circuit board are connected to associated electrodes of the semiconductor chip. The other surface of the printed circuit board includes an electrode connected to the electrodes on the one surface by the through-hole and the first and second electrodes provided in the respective vias for connection. The semiconductor device is connected to a mounting circuit substrate on the opposite surface of the printed circuit board.

[0019]

In a further aspect of the present invention, there is provided a method for producing a printed circuit board. The method comprises various steps as follows:

(a) a step of roughing the surface of a metal sheet which is to be a core

substrate;

(b) a step of forming a dielectric film of a capacitor on at least the roughed surface of the metal sheet;

(c) a step of forming a first electrically conductive layer on a dielectric film for a capacitor;

(d) a step of forming a second electrically conductive layer in an area on the surface of the first electrically conductive layer in register with an area in which a first via for electrical connection to the first electrically conductive layer is to be formed;

(e) a step of boring a hole through the first electrically conductive layer and the dielectric film of the capacitor in an area in which a second via for electrical connection to the metal sheet is to be formed to remove the first electrically conductive layer and the dielectric film of the capacitor to expose the metal sheet;

(f) a step of encapsulating an assembly including the metal sheet, said first electrically conductive layer, said dielectric film for the capacitor and the second electrically conductive layer, formed by the respective steps, with an electrically insulating resin;

(g) a step of boring through the resin in the first via for connection to expose the second electrically conductive layer and boring through the resin in the second via for connection to expose the metal sheet; and

(h) a step of depositing an electrically conductive material in a conductor pattern including the vias and in a through-hole.

[0020]

A method for producing a printed circuit board in another aspect of

the invention comprises

(a) a step of forming an insulating member in a partial area on the surface of a metal sheet, as a core substrate, where electrical connection to the metal sheet is to be established;

(b) a step of roughing the surface of the metal sheet as a partial area of the metal sheet is covered by the insulating member;

(c) a step of forming a dielectric film for a capacitor on the roughed surface of the metal sheet except an area thereof covered by the insulating member, while the insulating member is left on the metal sheet;

(d) a step of forming a first electrically conductive layer on the dielectric film for the capacitor while the insulating member is left on the metal sheet;

(e) a step of forming a second electrically conductive layer in an area of the surface of said first electrically conductive layer in which a first via for electrical connection to said first electrically conductive layer is to be formed, while said insulating member is left on said metal sheet;

(f) a step of encapsulating an assembly including the metal sheet, said first electrically conductive layer, said dielectric film for the capacitor and the second electrically conductive layer, with the insulating member, formed by the respective steps, with an electrically insulating resin;

(g) a step of boring in the resin in the first via for connection to expose the second electrically conductive layer and boring in the resin and the insulating member in the second via for electrical connection to the metal sheet, to expose a portion of the surface of the metal sheet; and

(h) a step of depositing an electrically conductive material in a conductor pattern including the vias.

[0021]

As may be seen from the foregoing explanation, the above object may similarly be accomplished by the claims and sub-claims.

BRIEF DESCRIPTION OF THE DRWINGS

Fig.1 is a cross-sectional view showing the structure of a first embodiment of the present invention at a typical cross section.

Figs.2A and 2B are enlarged partial views showing portions A and B in Fig.1.

Fig.3 is a cross-sectional view showing the structure of a second embodiment of the present invention at a typical cross section.

Figs.4A and 4B are enlarged partial views showing portions A and B in Fig.3.

Fig.5 is a cross-sectional view showing the structure of a third embodiment of the present invention.

Figs.6A and 6B are enlarged partial views showing portions A and B in Fig.5.

Fig.7 is a cross-sectional view showing the structure of a fourth embodiment of the present invention.

Fig.8 is a cross-sectional view showing the structure of a fifth embodiment of the present invention.

Figs.9A, 9B and 9C are cross-sectional views showing the manufacturing method of the first embodiment of the present invention, step-by-step.

Figs.10A and 10B are cross-sectional views showing the manufacturing method of the first embodiment of the present invention, step-by-step.

Figs.11A and 11B are cross-sectional views showing the manufacturing method of the first embodiment of the present invention, step-by-step.

Figs.12A, 12B and 12C are cross-sectional views showing the manufacturing method of the second embodiment of the present invention, step-by-step.

Figs.13A and 13B are cross-sectional views showing the manufacturing method of the second embodiment of the present invention, step-by-step.

Figs.14A and 14B are cross-sectional views showing the manufacturing method of the second embodiment of the present invention, step-by-step.

[0022]

PREFERRED EMBODIMENTS OF THE INVENTION

Now, certain embodiments of the present invention are hereinafter explained. The reference symbols mentioned herein relate to help understanding and are not intended to restrict anyhow the invention to embodiments as illustrated in the figures.

An embodiment of the present invention includes a metal sheet (11), the surface of which is partially or totally roughed to present micro-irregularities, a dielectric film for a capacitor (12), formed for covering at least the roughed surface of the metal sheet (11), presenting micro-

irregularities, and a first electrically conductive layer (13) formed for covering the roughed surface of the dielectric film for a capacitor (12), presenting micro-irregularities. The first electrically conductive layer (13) is formed of an electrically conductive high molecular (or polymer) layer which forms a solid electrolyte material of the cathode.

[0023]

In the present embodiment, a second electrically conductive layer (14) is formed on the surface of the first electrically conductive layer (13) in the region of a via for cathode side connection (18) for establishing electrical connection of the first electrically conductive layer (13).

[0024]

In the present embodiment, there is provided no dielectric film for the capacitor (12), nor the first electrically conductive layer (13), nor the second electrically conductive layer (14) on the metal sheet (11) in the region of the via for cathode side connection (19) for establishing electrical connection for the metal sheet (11).

[0025]

In the present embodiment, an electrically insulating resin (also termed an inter-layer resin layer) (15) exemplified, e.g., by epoxy resin is provided for covering the metal sheet (11), dielectric film for a capacitor (12) and the first and second electrically conductive layers (13, 14).

[0026]

In the present embodiment, the via for cathode side connection (18)

includes an electrode (20) produced on depositing an electrically conductive member of, for example, copper, as by plating, in a via formed on boring through the resin (15) until the second electrically conductive layer (14) is reached. In a region surrounding the cathode side electrode (20), the bottom of the resin (15) abuts against (adheres to) the second electrically conductive layer (14). The anode side connection via (19), obtained on boring through the resin (15) until the surface of the metal sheet (11) is reached, is provided with an electrode (21) deposited in the via.

[0027]

In the anode side connection via (19), in the present embodiment, the resin (15), charged into a space between the anode side electrode (21) and the first electrically conductive layer (13) in the vicinity of the anode side connection via (19) provides for electrical insulation between the anode side electrode (21) and the first electrically conductive layer (13) in the vicinity of the anode side connection via (19). The resin (15), having its bottom abutting against the metal sheet (11), surrounds a portion of the lateral surface of the anode side electrode (21).

[0028]

In the present embodiment, the metal sheet (11), dielectric material for a capacitor (12) and the first electrically conductive layer (13) make up a capacitor device, while the first electrically conductive layer (13), the second electrically conductive layer (14) for electrode contact and the electrode (20) make up the cathode side electrode. The metal sheet

(11) works as an anode, with the electrode (21) forming the anode side electrode.

[0029]

In the present embodiment, the dielectric material for the capacitor (12) is a metal oxide film. The electrically conductive high molecular layer, forming the first electrically conductive layer (13), is formed of at least one of, for example, polypyrrole, polythiophene and polyaniline.

[0030]

In the present embodiment, the second electrically conductive layer (14) is preferably of a dual film structure, e.g., composed of a carbon paste layer and a silver paste layer.

[0031]

In another embodiment of the present invention, an insulating member (22), having one surface contacting with the metal sheet (11), is provided surrounding the electrode (21) on the surface of the metal sheet (11) in the anode side connection via (19). The surface of an insulating member (22) opposite to the one surface in an upstanding (vertical) direction normal to the surface of the metal plate (11) is flush with or at a higher position than the surface of the first electrically conductive layer (13), and abuts against the resin (15). The insulating member (22), surrounding a portion of the lateral surface of the anode side electrode (21), provides for electrical insulation between the anode side electrode (21) and the first electrically conductive layer (13) lying in the vicinity of the anode side connection via (19). Preferably, the insulating member (22) is formed of a resist, operating as a mask for

roughing the surface of the metal plate (11), being left on the metal sheet (11).

[0032]

In a further embodiment of the present invention, the second electrically conductive layer, interposed between the first electrically conductive layer (13) and the cathode side electrode (20), may be formed by a metal plating layer provided for covering the first electrically conductive layer (13). The metal plating layer (13) is formed of a metal, e.g., which is one of nickel, copper and indium or an alloy thereof.

[0033]

The manufacturing method of the present invention comprises e.g., the following steps:

[0034]

Step 1: The surface of the metal plate (11), as a core substrate, is roughed, and a bore or bores is/are formed in a needed location(s) of the metal plate (11).

[0035]

Step 2: The dielectric film for a capacitor (12) is formed on the roughed surface of the metal sheet (11).

[0036]

Step 3: The first electrically conductive layer (13) is formed on the dielectric film for the capacitor (12). The first electrically conductive layer (13) is made up by an electrically conductive high molecular layer formed a cathode side solid electrolyte material.

[0037]

*Step 4: The second electrically conductive layer (14) is formed in a* region of the surface of the first electrically conductive layer (13) where a via for cathode side connection for establishing electrical connection to the first electrically conductive layer (13) is to be formed.

[0038]

*Step 5: A bore is formed through the regions of the first* electrically conductive layer (13) and the dielectric film for the capacitor (12) where the via (19) for anode side connection for establishing the connection (contact) to the metal sheet (11) is to be formed, thereby exposing the metal sheet (11).

[0039]

Step 6: The assembly including the metal sheet (11), dielectric film for the capacitor (12), first electrically conductive layer (13) and the second electrically conductive layer (14) is encapsulated by an electrically insulating resin (15).

[0040]

Step 7: Bores are formed through the resin (15) to form the first and second vias for connection (18, 19). At this time, the resin (15) is removed as far as the upper surface of the second electrically conductive layer (14) in the first via for connection to expose the second electrically conductive layer (14). In the second via for connection (19), a bore is formed through the resin (15) until the metal sheet (11) is exposed.

[0041]

Step 8: An electrically conductive material (16) is deposited in a conductor pattern including each via and in the through-hole.

[0042]

The manufacturing method for a printed circuit board, according to a further embodiment of the present invention, comprises e.g., the following steps:

[0043]

Step 1: An insulating member (22) is formed in a portion of the surface of the metal sheet (11) as a core substrate where electrical connection is to be established to the metal sheet.

[0044]

Step 2: Under the condition that the surface of the metal sheet (11) is covered with the insulating member (22), the surface of the metal sheet (11) is roughed. The insulating member (22) operates as a mask for the roughing processing, such that the surface of the metal sheet (11) not covered by the insulating member (22) is roughed, while the surface of the metal sheet (11) covered by the insulating member (22) is not roughed.

[0045]

Step 3: Leaving the insulating member (22) on the metal sheet (11), the dielectric film for the capacitor (12) is formed on the surface of the roughed metal sheet (11).

[0046]

Step 4: Leaving insulating member (22) is left on the metal sheet (11), the first electrically conductive layer (13) is formed on the

dielectric film for the capacitor (12). The first electrically conductive layer (13) is not formed on the insulating member (22).

[0047]

Step 5: Leaving the insulating member (22) on the metal sheet (11), the second electrically conductive layer (14) is formed in an area of the surface of the first electrically conductive layer (13) where the first via for connection (18) for setting electrical connection to the first conductor layer is to be formed. The second electrically conductive layer (14) is not formed on the insulating member (22).

[0048]

Step 6: The assembly including the metal sheet up to the second electrically conductive layer and the insulating member (22), formed by the above steps, is encapsulated by an electrically insulating resin (15).

[0049]

Step 7: At the first via for connection (18), a bore is formed through the resin (15) to expose the second electrically conductive layer (14). At the second via for connection (19) for setting electrical connection to the metal sheet (11), a bore is formed through the resin (15) and the insulating member (22) to expose a portion of the surface of the metal sheet (11).

[0050]

Step 8: An electrically conductive material is deposited according to a conductor pattern inclusive of each via.

[0051]

In the above-described embodiment of the further embodiment of

the present invention, the insulating member (22), which is to become a mask for the roughing processing, is pre-formed in a region of the surface of the metal sheet (11) in which the via for anode side connection is to be formed. In the roughing processing, the region covered by the insulating member (22) is not roughed, while neither the dielectric film for the capacitor (12) nor the first electrically conductive layer (13) is formed in this region. As a consequence, only one boring step by e.g., laser working in the above step 7 would suffice for forming the via for anode side connection, thus simplifying the manufacturing process for the printed circuit board of the buried capacitor type, insofar as the boring process is concerned.

[0052]

In a method of a still further embodiment of the present invention, the second electrically conductive layer (23) comprised of a metal plating is formed in step 5 to overlie the first electrically conductive layer (13) except the area of the insulating member (22). In step 7, a bore is formed through the resin (15) to form the via for cathode side connection and the via for anode side connection, respectively. In the via for cathode side connection, the resin (15) is removed as far as the upper surface of the second electrically conductive layer (23) is exposed. In the via for anode side connection, a bore is formed through the resin (15) and the insulating member (22) until the metal sheet (11) is exposed.

[0053]

Preferred Embodiments

For more detailed description of the above-described embodiments of the present invention, the embodiments of the present invention are now explained with reference to the drawings. Figs.1 and 2 illustrate the structure of a first embodiment of the present invention.

[0054]

An aluminum sheet (Al sheet) 11, forming a metal core substrate of the printed circuit board, has a roughed surface. Specifically, micro-irregularities are formed on the surface of the foil-shaped aluminum sheet 11 by e.g., etching. By employing a metal sheet, e.g., aluminum sheet 11 as a core substrate, it is possible to reduce the substrate thickness and yet to provide for the required strength.

[0055]

On the surface of the aluminum sheet 11, an aluminum oxide (Al oxide) layer 12, as a dielectric film for a capacitor, is formed to a thickness having e.g., hundreds of picometers (pm), where 1 pm is $10^{-12}$ m, as a lower limit and having e.g., tens of nanometers (nm) as an upper limit. The thin film of the aluminum oxide layer 12 may be formed by any suitable film-forming method, such as a sputtering method. Thus, in the present embodiment, an oxide film, formed by the aluminum oxide layer 12, having a high dielectric constant, is formed on the aluminum sheet 11, having a surface area increased by the roughing processing, whereby the capacitance of the capacitor is increased by reduction in the capacitor thickness and the enlarged electrode surface area.

[0056]

On the surface of the aluminum oxide layer 12, there is formed, as

a counter-electrode, a solid electrolyte layer, such as a layer of an electrically conductive high molecular material (e.g., polymer) 13. The thin film of the aluminum oxide layer 12 is coated by a solid electrolyte material, such as by the layer of an electrically conductive high molecular material 13, to provide for insulating properties. The layer of the electrically conductive high molecular material 13 is formed of, for example, polypyrrole, which is a polymeric pyrrole layer or the like. As disclosed in for example the Publication of the JP Patent Kokai JP-A-7-94368, such a solid electrolyte capacitor has been developed in which an electrically conductive high molecular compound, exhibiting electrical conductivity by doping a high molecular compound, having a conjugate system, such as polypyrrole, with a compound exhibiting electron donating or electron attracting properties, is used as a solid electrolyte material for a cathode. In the solid electrolyte capacitor, a layer of an electrically conductive chemical oxidation polymerization high molecular compound of polypyrrole, a graphite layer and a silver paste layer are formed on the surface of the dielectric oxide film in this order. In the present embodiment, the layer of an electrically conductive high molecular material 13 may be formed by e.g., polythiophene or polyaniline, etc. in place of polypyrrole.

[0057]

In the layer of an electrically conductive high molecular material 13, an electrically conductive paste 14 is formed as an electrically conductive electrode contact layer in a location of connection by a connection via (contact via) for the anode. This electrically

conductive paste 14 is of a dual layer structure comprised of a silver paste layer deposited on a carbon paste layer.

[0058]

These layers are encapsulated (sealed-in/sandwitched) by an insulating resin 15, such as epoxy resin. A through-hole (T/H) 17 extending throughout the resin 15, a cathode connecting via 18, formed by a blind via, and an anode connecting via 19, are then formed.

[0059]

This printed circuit board 10 has the aluminum sheet 11 as an anode (+) and, with interposition of the aluminum oxide layer 12, has the electrically conductive paste 14 as a cathode (-). The electrical charges are accumulated in the spacing in-between.

[0060]

This printed circuit board 10 includes a through-hole 17 and a pair of copper plating sites 16, on both the front and back surfaces of the board, electrically connected to the through-hole 17, thus assuring signal interconnections across the front and back surfaces.

[0061]

Meanwhile, the aluminum sheets 11A and 11B, shown in the cross-sectional view of Fig.1, are in unison (solid) with each other. When viewed from the upper side, the planar configuration of the aluminum sheets 11A and 11B may be of any desired optional pattern, such as annular or $\pi$ pattern.

[0062]

Figs.2A and 2B are enlarged partial cross-sectional views showing

an area A, shown encircled in Fig.1 (a cathode connection via 18 and its vicinity), and an area B (an anode connection via 19 and its vicinity), respectively.

[0063]

Referring to Fig.2A, the via for cathode connection includes an electrode 20, connected via electrically conductive paste 14 to the layer of the electrically conductive high molecular material 13, operating as a counter-electrode of the aluminum sheet 11. The aluminum oxide layer 12 is formed on the aluminum sheet 11, having the roughed surface, the layer of the electrically conductive high molecular material 13 is formed thereon, and the electrically conductive paste 14 is provided on the upper surface of the layer of the electrically conductive high molecular material 13. A hole (blind via) is bored in the encapsulating resin 15 by, for example is exposed laser irradiation, as deep as the electrically conductive paste 14 is exposed. The electrode 20 is formed by depositing an electrode material, such as copper, such as by plating.

[0064]

Referring to Fig.2B, there is formed no aluminum oxide layer nor a layer of an electrically conductive high molecular material in a via area for anode side connection for having contact with the aluminum sheet 11 on the surface of the aluminum sheet 11, but a hole (blind via) is bored in the resin 15, such as by laser irradiation, as deep as the surface of the aluminum sheet 11 is exposed, and an electrode material, such as copper, is deposited in the blind via by for example electroless plating to form the electrode 21. In depositing the electrode material, such as copper,

the electrode material, such as copper, is deposited conductor patterns (not shown) and in the inside of the through-hole 17 (see Fig.1).

[0065]

Referring to Fig.2B, showing the via for anode side connection, the resin 15 surrounding the lateral sides of the electrode 21 has its bottom in abutting contact (intimate adhesion) with the aluminum sheet 11. The electrical insulation between the anode side electrode 21 and the cathode side layer of the electrically conductive high molecular material 13 around the via for anode side connection is assured by the resin 15 introduced into the space between the electrode 21 and the layer of the electrically conductive high molecular material 13 around the via for anode side connection. By providing the aluminum oxide layer 12 and the layer of the electrically conductive high molecular material 13 up to the vicinity of the via for anode side connection, the capacitance of the capacitor may be increased, while the electrical insulation across the anode and the cathode may be secured by the resin 15.

[0066]

The surface roughness of the aluminum sheet 11 is e.g., 1 to 50 $\mu$ m (micrometers), i.e., above the micrometer order, while the film thickness of the aluminum oxide layer 12 is, e.g., hundreds of pm (several Angstroms) to (several) tens of nm. The film thickness of the polypyrrole film forming the layer of the electrically conductive high molecular material 13 is e.g., 10 to 50 $\mu$ m. The film thickness of the double-layer electrically conductive paste 14, composed of the carbon paste and the silver paste, is e.g., 5 to 20 $\mu$ m, while the film thickness

of the resin 15 is, e.g., 10 to 20 $\mu$ m.

[0067]

With the present embodiment, described above, the aluminum oxide layer 12 can be of an extremely reduced thickness, while the electrode surface area may be increased by the roughing processing of the aluminum sheet 11, while the polypyrrole film may be coated on the roughed surface of the aluminum sheet 11 with optimum follow-up characteristics, so that the counter-electrode of the aluminum sheet 11 can be increased in the surface area to realize a high capacitance. The capacitor of high capacitance may be realized, while the through-holes traversing the substrate are formed and a desired pattern is formed on the front and back surfaces of the substrate, so that the substrate may perform the role of an interposer.

[0068]

A second embodiment of the present invention is now explained. Referring to Fig.3, showing the structure of the second embodiment of the present invention, an insulating resin 22 is formed in the via for anode side connection, around the site of connection to the aluminum sheet 11, to provide for electrical insulation across the electrode 21 on the anode side and the cathode side.

[0069]

Figs.4A and 4B are enlarged partial cross-sectional views showing an area A shown encircled in Fig.3 (a cathode connection via 18 and its vicinity) and an area B (an anode connection via 19 and its vicinity), to an enlarged scale, respectively. The structure of the second

embodiment of the present invention differs from that of the above-described first embodiment only as to the via for anode side connection and is otherwise the same as the structure of the above-described first embodiment. That is, in the second embodiment of the present invention, the via for cathode side connection is similar in structure to that shown in Fig.2A. In the following, the via for anode side connection, by which the second embodiment differs from the above-described first embodiment, is explained.

[0070]

Referring to Fig.4B, on an aluminum board 11 there is formed no aluminum oxide layer nor a layer of an electrically conductive high molecular material in a via area for anode side connection, and a hole (blind via) is bored by, e.g., laser irradiation through the resin 15, until reaching the surface of the aluminum sheet 11, and an electrode material, such as copper, is deposited by for example electroless plating to form the electrode 21. An insulating resin 22 is deposited for laterally surrounding the bottom of the electrode 21 on the surface of the aluminum sheet 11 so that the insulating resin has its one surface in contact with the aluminum sheet 11. The opposite side surface of the insulating resin 22 has an elevated surface at a position vertically elevated from the aluminum sheet 11 flush with or higher in level than the layer of surface the electrically conductive high molecular material 13, and abuts against the resin 15 at the upper end of the insulating resin 22. The insulating resin 22 has its inner peripheral side surrounding a portion of the lateral side of the electrode 21, while having its outer

peripheral surface abutting against the layer of the electrically conductive high molecular material 13 forming the counter-electrode. The electrical insulation across the electrode on the anode side 21 and the cathode side may be maintained in this manner by the insulating resin 22 provided on the aluminum sheet 11 between the electrode 21 and the electrically conductive high molecular material 13 on the aluminum sheet 11.

[0071]

That is, in the second embodiment, the electrical insulation across the anode side electrode 21 and the layer of the electrically conductive high molecular material 13 is assured by the insulating resin 22.

[0072]

As this insulating resin 22, an etching resist, operating as a mask for roughing processing of the aluminum sheet 11, may also be used, as will be explained later on in connection with the explanation of the manufacturing method. The etching resist in this case is left over unchanged on the aluminum sheet 11 after the roughing processing (the etching resist is termed a [permanent resist]).

[0073]

Referring to Figs.3 and 4B, the area of the via for anode side connection on the surface of the aluminum sheet 11, and the near-by area where the insulating resin 22 is formed, are at a higher height level than the other peripheral area where there are provided the aluminum oxide layer 12 and the layer of the electrically conductive high molecular material 13, by way of providing a stepped structure. This stepped

structure is afforded by etching the aluminum sheet 11, in the course of the surface roughing process of the aluminum sheet 11, using the insulating resin 22 as a mask. The height of the step difference of the aluminum sheet 11 and the thickness of the insulating resin 22 are set so that the lateral side of the insulating resin 22 will overlie the bottom surface and the upper surface of the layer of the electrically conductive high molecular material 13. In the second embodiment, the film thicknesses of the aluminum oxide layer 12 and the layer of the electrically conductive high molecular material 13 are selected to be similar to those of the first embodiment described above. In the present second embodiment, the boring process of the via for anode side connection in the manufacture process for the printed circuit board is simplified.

[0074]

A third embodiment of the present invention is now explained. Fig.5 depicts the structure of the third embodiment of the present invention. Referring to Fig.5, the third embodiment of the present invention is similar to the second embodiment, explained with reference to Fig.3, except that the electrically conductive paste 14 is replaced by a metal plating layer 23. That is, in the present third embodiment, a layer of the electrically conductive high molecular material 13 of, for example, polypyrrole, is formed on the surface of the aluminum oxide layer 12, formed on the roughed surface of the aluminum sheet 11, the metal plating layer 23 is formed on the surface of the layer of the electrically conductive high molecular material 13, and a resin 15 is

formed on the metal plating layer 23. The metal plating layer is formed of nickel, copper or indium. The via for anode side connection, for assuring the contact with the aluminum sheet 11, has been removed on the metal plating layer 23. In the via for anode side connection, the insulating resin 22 is provided between the electrode 21 for the anode and the ends of the layer of the electrically conductive high molecular material 13 and the metal plating layer 23 for assuring electrical insulation.

[0075]

Figs.6A and 6B are enlarged partial cross-sectional views showing an area A shown encircled in Fig.5 (a cathode connection via section 18 and its vicinity) and an area B (an anode connection via section 19 and its vicinity), respectively. In the following, the points of difference from the above-described first and second embodiments are explained.

[0076]

Referring to Fig.6A, the via section for cathode side connection includes an electrode 20 comprised of an electrically conducting member deposited in a via formed on boring the resin as far as the metal plating layer 23.

[0077]

Referring to Fig.6B, the via section for anode side connection is not provided with the aluminum oxide layer 12 nor with the layer of the electrically conductive high molecular material 13. The metal plating layer 23 also is removed in an area of a via forming section for anode side connection. The via section for anode side connection is provided

with an electrode 21 comprised of an electrically conducting member deposited in a via formed on boring the resin 15, such as by laser working, as far as the aluminum sheet 11.

[0078]

In an area of the surface of the aluminum sheet 11, surrounding the bottom of the electrode 21, there is provided an insulating resin 22, having its one surface abutting against the aluminum sheet 11. The opposite side surface of the insulating resin 22 has an upstanding position from the surface of the aluminum sheet 11 flush with or at a higher height level than the metal plating layer 23 in the vicinity of the via for anode side connection, and is abutted against the resin 15. The insulating resin 22 has its inner peripheral surface surrounding a portion of the lateral surface of the electrode 21, while having its outer peripheral surface abutting against the ends of the metal plating layer 23 and the layer of the electrically conductive high molecular material 13.

[0079]

Thus, in the present third embodiment of the present invention, the electrical insulation between the electrode 21 of the anode and the cathode side by the insulating resin 22 provided between the electrode 21 on one hand and the metal plating layer 23 and the layer of the electrically conductive high molecular material 13 on the other hand is assured. That is, the electrical insulation between the anode electrode 21 on one hand and the metal plating layer 23 and the layer of the electrically conductive high molecular material 13 on the other hand is assured by the insulating resin 22.

[0080]

As this insulating resin 22, an etching resist, operating as a mask for roughing processing of the aluminum sheet 11, may also be used, as will be explained later on in connection with the explanation of the manufacturing method. The etching resist in this case is left over unchanged on the aluminum sheet 11 after the roughing processing.

[0081]

The area of the via for anode side connection on the surface of the aluminum sheet 11, and the near-by area where the insulating resin 22 is formed, is at a higher level than the other peripheral area where there are provided the aluminum oxide layer 12 and the layer of the electrically conductive high molecular material 13, by way of providing a stepped structure. This stepped structure is afforded by etching the aluminum sheet 11, in the course of the surface roughing process of the aluminum sheet 11, using the insulating resin 22 as a mask. It is noted that the film thicknesses of the aluminum oxide layer 12 and the layer of the electrically conductive high molecular material 13 are the same as those of the above-described first embodiment.

[0082]

A fourth embodiment of the present invention is now explained. Fig.7 depicts the structure of the fourth embodiment of the present invention. Fig.7 schematically shows the cross-section of a mounting structure in which a semiconductor device, such as CSP (chip size package), provided with the printed circuit board 10 of the aforementioned first embodiment, is mounted on a circuit substrate

(motherboard) 130

[0083]

In the fourth embodiment of the present invention, shown in Fig.7, the printed circuit board 10, operating as an interposer, includes the aluminum sheet 11, as a core substrate, an aluminum oxide layer 12 and a layer of the electrically conductive high molecular material 13. The printed circuit board 10 includes, in a contact via section on the cathode side, an electrically conductive paste and an electrode 20 deposited in the via reaching the electrically conductive paste. The printed circuit board 10 also includes, on an anode side contact via 19, an electrode 21 deposited in the via reaching the aluminum sheet 11, and a layer of an encapsulating resin 15. The printed circuit board 10 is provided with a plated through-hole 17. Bumps of LSI 110 are soldered by, for example a flip chip method, to electrode pads (land of a through-hole or a via pad) provided by the face-down system on one surface of the printed circuit board 10. Solder bumps 24 are provided in a grid configuration to the opposite side surface of the printed circuit board 10. A solder resist or a mold resist is charged into a space between the printed circuit board 10 and the LSI 110 to form a CSP semiconductor device of the flip chip ball grid array (BGA) type. The electrodes 20, 21 of the connection vias 18, 19 of the cathode and the anode on one surface of the printed circuit board 10 are connected to for example a power supply terminal 112 and to a grounding terminal (bump) 111, while the land of the through-hole 17 of the printed circuit board 10 is connected to a signal terminal (bump) 113 of the LSI 110. The BGA (ball grid array)

of the CSP is soldered to the circuit substrate 130. On the opposite side surface of the printed circuit board 10, electrode bumps 105 of the connection vias of the anode and the cathode are connected to a power supply pad and a ground pad of the circuit substrate (motherboard) 130. The semiconductor device, mounted on the circuit substrate 130, is sealed by an encapsulating resin 120.

[0084]

The electrodes 20, 21, as contact electrodes for the capacitor enclosed in the printed circuit board 10, are connected to a near-by terminal of the LSI 110. Thus, the capacitor may be applied to a capacitor as a decoupling capacitor and a noise filter in the high speed high frequency LSI 110. Of course, the semiconductor device, provided with the printed circuit board according to the instant invention as an interposer (package substrate) is not limited to the flip chip ball grid array (BGA) type semiconductor device.

[0085]

A fifth embodiment of the present invention is now explained. Fig.8 shows the structure of a fifth embodiment of the present invention. Fig.8 shows the structure in which the printed circuit board of the first embodiment shown in Fig.1 is applied to a multi-layered printed circuit board. The fifth embodiment, shown in Fig.8, includes an aluminum sheet 11, as a core substrate, an aluminum oxide layer 12, as a dielectric film for a capacitor, and a layer of the electrically conductive high molecular material 13. The fifth embodiment also includes, in a contact via section on the cathode side, an electrically conductive paste

14, while including, on the cathode side contact via section 18, an electrode 20 reaching the electrically conductive paste 14. The anode side connection via 19 reaches the aluminum sheet 11 and is provided with an electrode 21. An interconnection layer (or layers) is(are) formed between the inter-layer insulating layers 15A and 15B and between the inter-layer insulating layers 15B and 15C. A cathode side connection via 18 and an anode side connection via 19 are provided as uppermost layers. On the opposite surface (back surface), there are provided a cathode side connection via 18A and an anode side connection via 19A. An electrode 20A of the cathode side connection via 18A on the back surface is connected to the electrically conductive paste 14 of the uppermost layer via a pattern of the interconnection layer and the through-hole, while the electrode 21A of the anode side connection via 19A is connected to the aluminum sheet 11 as the uppermost layer via a pattern of the interconnection layer and the through-hole. Although Fig.8 shows three-layered interconnections, it is not limitative of the present invention.

[0086]

The manufacturing method for the printed circuit board of the above-described embodiment of the present invention is now explained. Figs.9 to 11 schematically show the cross-section of the printed circuit board of the above-described first embodiment of the invention by way of illustrating the main manufacturing process step-by-step. It is noted that Figs.9 and 10 are split only for convenience in formulating the drawings.

[0087]

Referring to Fig.9A, a hole is bored at a desired location in a foil-shaped aluminum sheet 11 by e.g., drilling to form a through-hole 9.

[0088]

The surface of the aluminum sheet 11 is etched for forming micro-irregularities therein. The surface roughness is on the order of e.g., 1 to 50 $\mu$m.

[0089]

On the surface of the aluminum sheet 11, an aluminum oxide layer 12 is formed as a dielectric film, as shown in Fig.9B, to a film thickness of e.g., hundreds of pm to tens of nm. The capacitance is increased by formation of an oxide film as a dielectric film on the aluminum surface the surface area of which has been increased by roughing.

[0090]

A polypyrrole film, as a electrically conductive high molecular layer 13, then is formed on the aluminum oxide layer 12, to a film thickness of e.g., 10 to 50 $\mu$m, as shown in Fig.9C.

[0091]

The electrically conductive paste 14 is then formed in a location of the electrically conductive high molecular layer 13 (polypyrrole film) where the cathode contact via is to be formed, as shown in Fig.10A. This electrically conductive paste is made up of two layers, namely a carbon paste layer and a silver paste layer. The film thickness of the electrically conductive paste 14 is e.g. 5 to 20 $\mu$m.

[0092]

In a location of the electrically conductive high molecular layer 13 where an anode side connection via forming area is to be formed, boring for setting electrical connection to the aluminum sheet 11 is done by e.g., laser working, as shown in Fig.10B. The layers of polypyrrole and aluminum oxide are then removed to expose the grounding surface of the aluminum sheet 11.

[0093]

A resin film is then bonded to each of the upper and lower surfaces, as shown in Fig.11A, and the resin 15 is formed by vacuum laminating press. The film thickness of the resin 15 is set e.g., to 10 to 20 $\mu$m.

[0094]

On a site of the resin 15 where a through-hole is to be formed, a pre-hole 17a for the through-hole is formed, as shown in Fig.11B. A pre-hole 18a for connection (contact) on the cathode side and a pre-hole 19a for connection (contact) on the anode side are also formed e.g., by laser working.

[0095]

In the pre-hole 18a for connection on the cathode side, the resin 15 is removed up to the upper surface of the electrically conductive paste 14 to expose the electrically conductive paste 14.

[0096]

The pre-hole 19a for connection on the anode side is formed by laser working until the aluminum sheet 11 is exposed. It is noted that the diameter of the pre-hole 19a for connection on the anode side is smaller than the diameter achieved in the boring step shown in Fig.10B.

[0097]

For augmenting the plating bonding strength, the surface of the thermosetting insulating resin, such as epoxy resin, is chemically roughed, and a catalyst is applied to the surface and into the inside of the via to provide catalyst followed by formation of a plating resist, not shown. The electroless plating is then carried out to precipitate copper (16 of Fig.1) to form a conductor pattern and a plating through-hole (17 of Fig.1). The copper plating 16 is of a thickness of 5 to 25 $\mu$m.

[0098]

The above process completes the printed circuit board shown in Fig.1. As the through-hole plating technique, in which the patterns of interconnections on both surfaces are interconnected by through-hole plating, an additive method, for example, is used. However, this technique is merely illustrative and is not intended to limit the present invention thereto.

[0099]

The manufacturing method for the printed circuit board of the above-described second embodiment of the present invention, shown in Figs.3 and 4, is now explained. Figs.12 to 14 schematically show the cross-section of the printed circuit board of the above-described second embodiment of the invention by way of illustrating the main manufacturing process step-by-step. It is noted that Figs.12 to 14 are split only for convenience in formulating the drawings.

[0100]

Referring to Fig.12A, a hole is bored at a desired location in a

foil-shaped aluminum sheet 11 by e.g., drilling to form a through-hole.

[0101]

The insulating resin 22 is formed in a location of the surface of the aluminum sheet 11 where the contact to the aluminum sheet 11 is to be established, as shown in Fig.12B. The insulating resin (resist) 22 is formed prior to surface roughing of the aluminum sheet 11. As the insulating resin 22, an epoxy resin or a polyimide resin may be used. As the insulating resin 22, a modified photosensitive epoxy resin, or a photosensitive solder resist (PSR4000 NAS-90-TY, manufactured by TAIYO INK SEIZO KK or DSR 2200 BGX-8, manufactured by TAMURA KAKEN, for example, may be used.

[0102]

The surface roughing processing for the aluminum sheet 11 is then carried out, using this insulating resin 22 as a mask. This roughing processing is by etching, as an example. In this case, the surface area of the aluminum sheet 11 other than its surface coated by the insulating resin 22 is roughed to form micro-irregularities. Of course, the surface of the aluminum sheet 11 coated with the insulating resin 22 is not roughed.

[0103]

The aluminum oxide layer 12 then is formed, as a dielectric film for a capacitor, so as to follow up with the micro-irregularities of the roughed surface of the aluminum sheet 11, as shown in Fig.12C. The film thickness of the aluminum oxide layer 12 is hundreds of pm to tens of nm. Since an oxide film forming a dielectric film has been formed

on the aluminum sheet, the surface area of which has been enlarged by roughing processing, the capacitance value is increased. The aluminum oxide layer 12 is not formed on the surface area of the aluminum sheet 11 coated with the insulating resin 22.

[0104]

The polypyrrole film, as a layer of the electrically conductive high molecular material (polymer) 13, is then formed on the aluminum oxide layer 12, as shown in Fig.13A. The film thickness of the polypyrrole film is 10 to 20 $\mu$m. The polypyrrole film is not formed on the surface area of the aluminum sheet 11 coated with the insulating resin 22. The lateral surface of the insulating resin 22 abuts against the end of the polypyrrole film 13.

[0105]

The electrically conductive paste 14 is then formed in a location of the layer of the electrically conductive high molecular material (polypyrrole film) 13 where the cathode contact via is to be formed, as shown in Fig.13B. This electrically conductive paste is of a dual layer structure comprised of a carbon paste layer and a silver paste layer.

[0106]

A resin film then is bonded to each of the upper and lower surfaces, as shown in Fig.14A, to form the resin 15 by vacuum laminated press working.

[0107]

A pre-hole (basic hole)17a for a through-hole is then formed in a location of the resin 15 where the through-hole is to be formed. Pre-

hole 18a for the cathode side connection (contact) and pre-hole 19a for connection on the anode side are then formed by for example laser working.

[0108]

In forming the pre-hole 18a for connection on the cathode side, the resin 15 is removed up to the upper surface of the electrically conductive paste 14 to expose the electrically conductive paste 14.

[0109]

In boring the pre-hole 19a for connection on the anode side, a bore is formed in the resin 15 and in the insulating resin 22 to expose a portion of the surface of the site of the step difference of the aluminum sheet 11.

[0110]

For augmenting the plating adhesion properties, the surface of the thermosetting insulating resin, such as epoxy resin, is chemically roughed, and a catalyst(s) is applied to the surface and into the inside of the via to provide catalyst followed by formation of form a plating resist, not shown. The electroless plating is then carried out to precipitate copper (16 of Fig.3) to form a conductor pattern and a through-hole (17 of Fig.3). The above process completes the printed circuit board shown in Fig.3. As the through-hole plating technique, in which the patterns of interconnections on both surfaces are interconnected by through-hole plating, an additive method, for example, is used. This technique is merely illustrative and is not intended to limit the present invention thereto, as described above.

[0111]

In the manufacturing method of the present embodiment, the insulating resin (resist) 22, as a mask for roughing processing, is formed in the surface area of the aluminum sheet 11 where the via for anode side connection 19 is to be formed. In the roughing processing, this surface area is not roughed, while neither the aluminum oxide layer 12 nor the layer of the electrically conductive high molecular material (polypyrrole film) 13 is formed.

[0112]

Thus, in forming the via for anode side connection, only one boring operation by e.g., laser working suffices, thus simplifying the manufacture process for the preparation of the enclosed capacitor type printed circuit board.

[0113]

A third embodiment of the manufacturing method for a printed circuit board according to the present invention, shown in Figs.5 and 6, is now explained. In the manufacturing method for the printed circuit board according to the third embodiment of the present invention, after forming the polypyrrole layer 13, as a layer of the electrically conductive high molecular material, operating as a counter-electrode, on the aluminum oxide layer 12, by the process of Fig.13A, the metal plating layer 23 (see Figs.5 and 6) is formed in the process of Fig.13B, in place of forming the electrically conductive paste layer.

[0114]

A pre-hole on the cathode side then is formed in the process step of

Fig.14B. In this case, the hole is bored by laser working until the metal plating layer 23 is exposed. In forming the pre-hole 19a for connection on the anode side, a bore is formed in the resin 15 and in the subjacent insulating resin layer 22, with the laser working until the aluminum sheet 11 is exposed. This forms a pre-hole for connection on the anode side of the structure shown in Fig.6B (the electrode 21 of Fig.6B has not as yet been deposited in this process step). The manufacturing process is otherwise the same as the manufacturing process for the printed circuit board of the first embodiment described above.

[0115]

In the above-described manufacturing process for the printed circuit board of the present embodiment, the enclosed capacitor type printed circuit board can be produced, as the conventional process for manufacturing the printed circuit board is exploited, thereby reducing rise in the production cost to a minimum.

[0116]

With the above-described manufacturing method of the present invention, a capacitor of a high capacitance value may be formed in the substrate without obstructing the laying of the interconnections of the printed circuit board.

[0117]

Although the present invention has been described in the foregoing with reference to certain preferred embodiments thereof, the present invention is not limited to these particular embodiments and may

comprise various changes or modifications that may occur to those ordinarily skilled in the art within the scope of the invention defined in the appended claims.

[0118]

The meritorious effects of the present invention are summarized as follows.

The present invention, described above, gives rise to the following advantages:

[0119]

With the printed circuit board of the present invention, the electrode surface is roughed to increase its area, the oxide film having a high dielectric constant is formed to a reduced thickness, and the electrode-to-electrode distance is diminished to realize a printed circuit board having a capacitor of a large capacitance value enclosed therein. According to the present invention, it is possible to have a capacitor of a large capacitance value enclosed in a substrate of e.g., an interposer.

[0120]

Moreover, with the printed circuit board of the present invention, the electrical insulation across the anode electrode and the cathode electrode is maintained, such that a capacitor of a high capacitance value may be formed within the substrate, as the degree of freedom in designing is maintained, without inconvenience in laying the interconnections in the printed circuit board.

[0121]

Additionally, with the semiconductor device of the present

invention, it is possible to provide a package having enclosed therein a decoupling capacitor, a noise filter or a large capacitance capacitor array.

[0122]

With the manufacturing method of the present invention, a printed circuit board of the type having an enclosed capacitor can be produced, as the conventional manufacturing process for the printed circuit board is utilized, to render it possible to suppress the manufacturing cost of the printed circuit board of the type having an enclosed capacitor.

[0123]

Moreover, with the manufacturing method of the present invention, the insulating member, operating as a mask for roughing processing, is formed in an area in a metal sheet, in which to form the via for anode side connection. Since this area is not roughed, while neither the dielectric film for a capacitor nor a layer of an electrically conductive high molecular layer is formed in this area, the boring step needs to be carried out only once in forming the via for anode side connection, thereby simplifying the manufacture process for the printed circuit board of the type having an enclosed capacitor.

It should be noted that other objects, features and aspects of the present invention will become apparent in the entire disclosure and that modifications may be done without departing the gist and scope of the present invention as disclosed herein and claimed as appended herewith.

Also it should be noted that any combination of the disclosed and/or claimed elements, matters and/or items may fall under the

modifications aforementioned.